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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,466	10/31/2000	Shunpei Yamazaki	0756-2222	8851

31780 7590 03/22/2004

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EXAMINER	
SARKAR, ASOK K	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/699,466	Applicant(s) YAMAZAKI ET AL.	
	Examiner Asok K. Sarkar	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 35-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 35-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/784,290.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03; 12/5/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	09/699,466	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

All Participants:

(1) *Asok K. Sarkar*.

(2) *Eric J. Robinson*.

Status of Application: *Non-Final Rejection*

(3) _____.

(4) _____.

Date of Interview: *2 March 2004*

Time: _____

Type of Interview:
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description: .

Part I.

Rejection(s) discussed:
N/A

Claims discussed:
N/A

Prior art documents discussed:
References provided on IDS filed 10/27/03 and 12/5/2003

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
Applicant was requested to provide evidence that the references provided in the above mentioned IDSs were commonly owned by the Applicant. Applicant agreed to provide the evidence.

Part III.

- ☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.
- ☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

Asok Kumar Sarkar
(Examiner/SPE Signature) 3/5/2004

(Applicant/Applicant's Representative Signature – if appropriate)

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 27, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 – 3, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651 and Takeuchi, US 5,661,056.

Regarding claims 1 and 43, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to 50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;

- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa fails to teach: 1) performing a plasma treatment to the semiconductor Island and 2) forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide.

Regarding element 1, Nishikawa teaches plasma treatment for the benefit of removing the organic resist contaminants from semiconductor device surfaces in column 1, lines 5 – 17. Similarly, Otsubo teaches plasma treatment for the benefit of removing foreign particles from semiconductor surface (see Abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a plasma treatment to the semiconductor island for the benefit of removing the organic resist contaminants and other foreign contaminants that remains on the surface of the semiconductor device as taught by Nishikawa in column 1, lines 5 – 17 and Otsubo in the Abstract of the disclosure.

Regarding element 2, Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi.

Regarding claim 2, Suzawa teaches the semiconductor film is a crystalline semiconductor film as described above in rejecting claim 1.

Regarding claim 3, Suzawa teaches patterning by an isotropic dry etching method in between column 5, line 61 and column 6, line 13.

Regarding claims 46 and 49, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only

6. Claims 36, 38, 41, 44, 47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo,

US 5,531,862; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Guldi, US 5,535,471 and Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Chapter 4, last paragraph of page 274(1990).

Regarding claims 36, 38, 41 and 44, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to 50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa fails to teach: 1) performing a plasma treatment to the semiconductor island and 2) forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide using mixed gases of TEOS and N_2O.

Regarding element 1, Nishikawa teaches plasma treatment for the benefit of removing the organic resist contaminants from semiconductor device surfaces in column 1, lines 5 – 17. Similarly, Otsubo teaches plasma treatment for the benefit of removing foreign particles from semiconductor surface (see Abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a plasma treatment to the semiconductor island for the benefit of removing the organic resist contaminants and other foreign contaminants that remains on the surface of the semiconductor device as taught by Nishikawa in column 1, lines 5 – 17 and Otsubo in the Abstract of the disclosure.

Regarding element 2, Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Guldi teaches silicon oxide nitride can be deposited by using TEOS in column 1, lines 35 – 38, TEOS is the Si source.

Wolf teaches that silicon oxide nitride can be deposited using N_2O as the source for nitrogen in the last paragraph of page 274.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi. For forming the gate insulating film of silicon oxide nitride mixed gases of TEOS and N_2O can be used as taught by Guldi and Wolf for the Si and the N sources.

Regarding claims 47 and 50, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only.

7. Claims 35 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Yanagisawa, US 4,759,610 and Okushiba, US 5,902,993.

Suzawa teaches most limitations of these claims as described earlier in rejecting claims 1 and 43. Suzawa also teaches forming an interlayer insulating film 611 of silicon nitride over the gate electrode 610 (Fig. 6D) with reference to Fig. 6E in column 9, lines 6 – 8. However, Suzawa fails to teach forming a resin material layer over the interlayer insulating film 611.

Yanagisawa teaches TFT containing display devices in which insulating films can also be formed of an organic material (resin) in column 5, line 16.

Okushiba teaches that the resin materials provide excellent transparency and environmental protection in column 21, lines 25 – 32.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a resin material layer over the interlayer insulating film as taught by Yanagisawa in column 5, line 16. The motivation for adding a second resin layer will be to provide additional insulation and environmental protection for the electrode as taught by Okushiba in column 21, lines 25 – 32.

8. Claims 37, 39, 42, 45, 48 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Yanagisawa, US 4,759,610 and Okushiba, US 5,902,993.

Regarding claims 37, 39, 42 and 45, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to 50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;

- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- forming an interlayer insulating film 611 of silicon nitride with reference to Fig. 6E in column 9, lines 6 – 8.
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa fails to teach: 1) performing a plasma treatment to the semiconductor island, 2) forming a resin material layer over the interlayer insulating film and 3) forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide.

Regarding element 1, Nishikawa teaches plasma treatment for the benefit of removing the organic resist contaminants from semiconductor device surfaces in column 1, lines 5 – 17. Similarly, Otsubo teaches plasma treatment for the benefit of removing foreign particles from semiconductor surface (see Abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a plasma treatment to the semiconductor island for the benefit of removing the organic resist contaminants and other foreign contaminants that remains on the surface of the semiconductor device as

taught by Nishikawa in column 1, lines 5 – 17 and Otsubo in the Abstract of the disclosure.

Regarding element 2, Yanagisawa teaches TFT containing display devices in which insulating films can also be formed of an organic material (resin) in column 5, line 16.

Okushiba teaches that the resin materials provide excellent transparency and environmental protection in column 21, lines 25 – 32.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a resin material layer over the interlayer insulating film as taught by Yanagisawa in column 5, line 16. The motivation for adding a second resin layer will be to provide additional insulation and environmental protection for the electrode as taught by Okushiba in column 21, lines 25 – 32.

Regarding element 3, Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by

Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi.

Regarding claims 48 and 51, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only.

9. Claims 52 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651 and Takeuchi, US 5,661,056 as applied to claims 1 and 43 above and further in view of Mori, US 6,006,763.

Suzawa in view of Nishikawa, Otsubo, Masumo and Takeuchi teaches using oxygen plasma to remove organic impurities but fails to teach reducing and vaporizing them with hydrogen plasma.

Mori teaches a method of surface cleaning using both oxygen and hydrogen plasma for the benefit of efficiently cleaning a substrate surface for further processing in descriptions of columns 1 and 2.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to modify Suzawa's method in view of Nishikawa, Otsubo, Masumo and Takeuchi and use oxygen plasma to remove organic impurities by oxidizing and then reducing and vaporizing them with hydrogen plasma for the benefit of efficiently cleaning the substrate surface for further processing as taught by Mori in descriptions of columns 1 and 2.

10. Claims 53, 55, 57 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Guldi, US 5,535,471 and Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Chapter 4, last paragraph of page 274(1990) as applied to claims 36, 38, 41 and 44 above and further in view of Mori, US 6,006,763.

Suzawa in view of Nishikawa, Otsubo, Masumo, Takeuchi, Guldi and Wolf teaches using oxygen plasma to remove organic impurities but fails to teach reducing and vaporizing them with hydrogen plasma.

Mori teaches a method of surface cleaning using both oxygen and hydrogen plasma for the benefit of efficiently cleaning a substrate surface for further processing in descriptions of columns 1 and 2.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method in view of Nishikawa, Otsubo, Masumo, Takeuchi, Guldi and Wolf and use oxygen plasma to remove organic impurities by oxidizing and then reducing and vaporizing them with hydrogen plasma for

the benefit of efficiently cleaning the substrate surface for further processing as taught by Mori in descriptions of columns 1 and 2.

11. Claims 54, 56, 58 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Yanagisawa, US 4,759,610 and Okushiba as applied to claims 37, 39, 42 and 45 above and further in view of Mori, US 6,006,763.

Suzawa in view of Nishikawa, Otsubo, Masumo, Takeuchi, Yanagisawa and Okushiba teaches using oxygen plasma to remove organic impurities but fails to teach reducing and vaporizing them with hydrogen plasma.

Mori teaches a method of surface cleaning using both oxygen and hydrogen plasma for the benefit of efficiently cleaning a substrate surface for further processing in descriptions of columns 1 and 2.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method in view of Nishikawa, Otsubo, Masumo and Takeuchi and use oxygen plasma to remove organic impurities by oxidizing and then reducing and vaporizing them with hydrogen plasma for the benefit of efficiently cleaning the substrate surface for further processing as taught by Mori in descriptions of columns 1 and 2.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1 – 3 and 35 – 51 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 38 of U.S. Patent No. 6,180,439 B1 in view of Suzawa, US 5,728,259; Nishikawa, US 5,575,883; Otsubo, US 5,531,862; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Guldi, US 5,535,471; Mori, US 6,006,763 and Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Chapter 4, last paragraph of page 274(1990) and Yanagisawa, US 4,759,610.

Most limitations of these claims such as forming semiconductor film, crystallizing the film by first heating, patterning the film to an island/mesa shape, laser irradiating the semiconductor film, forming gate insulating film of silicon oxide are taught by the claims of Patent No. 6,180,439 B1.

Other aspects of the claims such as plasma treatment, forming a second gate insulating film of silicon oxide nitride by reacting TEOS with N_2O, forming an interlayer insulating film of silicon nitride, covering it with a resin material, forming the gate, source and drains are covered by the additional references as were described earlier in rejecting these claims under 35 U.S.C. 103(a).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
3/5/2004

Asok K. Sarkar
March 5, 2004

Patent Examiner